Attorney Docket No. 00-LM-117
Client/Matter No. 80408.00063
VIA EFS-WEB

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:	Confirmation No. 9379
Wen Lin	Art Unit: 2189
Serial No.: 09/943,242	Examiner: Woo H. Choi
Filed: August 30, 2001	Customer No. **30429**
For: **INTEGRATED DRIVE CONTROLLER FOR SYSTEMS WITH INTEGRATED MASS STORAGE**	Docket No. 00-LM-117

Mail Stop Appeal Brief - Patents
Commissioner for Patents
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Alexandria, VA 22313-1450

APPEAL BRIEF UNDER 37 CFR § 41.37

I. Real Party in Interest

STMicroelectronics, Inc.
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II. Related Appeals and Interferences

No other appeals or interferences are currently known to Appellant that will directly affect, be directly affected by, or have a bearing on the decision to be rendered by the Board of Patent Appeals and Interferences in the present appeal.

III. Status of Claims

Claims 1-3, 5, 7, 10, 12, 17-22, and 32 are pending in the application, with claims 4, 6, 8, 9, 11, 13-16, and 23-31 being cancelled. No claims have been allowed, and all pending claims stand rejected under 35 U.S.C. §102 or §103. The rejection of claims 1-3, 5, 7, 10, 12, 17-22, and 32 is the subject of this appeal.

IV. Status of Amendments

The Advisory Action indicates that the claim amendment filed subsequent to the final Office Action of February 10, 2006 was entered and overcame all rejections under 35 U.S.C. §112. Hence, all claim amendments have been entered.

Claims 1-3, 5, 7, 10, 12, 17-22, and 32 are provided in the attached Claims Appendix in their amended state.

V. Summary of Claimed Subject Matter

Claims 1 and 32 are independent claims that are being appealed.

Claim 1 is directed to a computing system such as the exemplary system shown in Figure 2 of Appellant's specification. The computing system of claim 1 includes a processor with a data/control bus interface 100 shown interfacing with a "local bus." The system includes a mass storage device such as devices 204A, 204B, 204C and data memory such as system memory 411. Significantly, the computing system of claim 1 includes "a bus controller" such as controller 201 of Figure 2 that has "a memory interface" coupled to the data memory 411 and "a mass storage interface coupled to the mass storage device's interface without an intermediary mass storage controller." For example, this may be seen with the "PCI I/F" coupled via PCI bus to "PCI I/F" of mass storage device 204C. The feature of "without an intermediary mass storage controller" can be further understood by studying the prior art system of Figure 1 in which mass storage controllers 103 are provided between the bus controller 101 and mass storage devices 104. In contrast, the mass storage controller 201 of Figure 2 couples directly to the mass storage devices 204 without such an intermediary mass storage controller and its additional interfaces/hardware

and according to claim 1 is "operable to conduct mass storage transactions between the data memory and the mass storage device" and to perform arbitration operations. Accordingly, the system of claim 1 is addressing problems noted in Appellant's Background such as at paragraph [0007] associated with the failure of bus interface and network technology to advance along with the speed of processors and to require multiple software and hardware layers and often utilizing slower busses to access mass storage devices.

The exemplary components of claim 1 shown in Figure 2 are described in detail beginning at paragraph [0028] of Appellant's specification. As noted in paragraph [0029], a "significant feature of the present invention is that mass storage mechanisms 204A, 204B, 204C are coupled to upstream busses and connections so as to eliminate one or more interface crossings that occur in the conventional implementation of Fig. 1." Further, in paragraph [0030], the mass storage devices are said to "couple directly" to busses such as the PCI bus without the need for the ATA I/F interface mechanisms shown in the prior art system of Figure 1 or as indicated in claim 1, the bus controller has a mass storage interface coupled to the mass storage device's interface "without an intermediary mass storage controller."

Independent claim 32 includes several limitations similar to those of claim 1, and the brief summary of like features and components of claim 1 is applicable to claim 32. However, claim 32 includes several limitations or elements not called for in claim 1. Claim 32 is directed to a computing system calls for a processor that "implements mass storage control processes to control the mass storage device." With the example of the system of Figure 2, the microprocessor 100 is shown to implement mass storage control processes 201. In paragraph [0028], it is stated "In contrast to the implementation of Fig. 1, the main processor 100 is preferably used to implement mass storage control processes" and these processes are described as implementing "some or all of the behaviors previously implemented within mass storage controller 103 and the interface of mass storage controller 103 and the interface of mass storage mechanisms 104."

Claim 32 also calls for particular interfacing and coupling not required in claim 1. For example, claim 32 calls for a first mass storage device with an interface and first mass storage

device is coupled to a data/control bus, which may be seen with mass storage device 204A and its local bus I/F coupled to local bus (e.g., claim 1 does not call for this "first mass storage device"). In claim 32, a processor is coupled to this same bus, which may be seen with microprocessor 100 coupled to local bus in the system of Figure 2. As with claim 1, a second mass storage device is coupled via its interface (see, device 204A and its PCI I/F) to a bus controller with its mass storage interface (see bus control 201 with PCI I/F in Figure 2). Claim 32 also calls for the data memory (such as system memory 411) to be coupled to the data/control bus and for the bus controller to conduct mass storage transactions between the data memory and the second mass storage device (e.g., between device 204C and system memory 411). Hence, claims 1 and 32 have some common elements, but claim 32 includes a number of limitations that differ from claim 1. These additional limitations, of course, need to be considered fully when examining the allowability of claim 32.

VI. Grounds of Rejection to be Reviewed on Appeal

Claims 1-3, 5, and 21 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Pat. Publ. No. 2003/0037198 ("Hunsaker").

Claims 1, 12, and 20 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Pat. No. 6,601,126 ("Zaidi").

Claims 1, 14, and 20 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Pat. No. 6,128,669 ("Moriarty").

Claims 1 and 19 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Pat. Publ. No. 2002/0144121 ("Ellison").

Claims 17 and 18 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Pat. No. 6,493,656 ("Houston").

Claims 7, 10, and 32 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Hunsaker, Zaidi, Moriarty, or Houston in view of "Operating Systems: Design and Implementation" by Andrew S. Tanenbaum ("Tanenbaum").

Claim 22 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Hunsaker in view of U.S. Pat. Publ. No. 2003/0181205 ("Yiu").

VII. Argument

Rejection of Claims 1-3, 5, and 21 Under 35 U.S.C. §102 Based on Hunsaker Is Improper

In the February 10, 2006 Final Office Action, claims 1-3, 5, and 21 were rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Pat. Publ. No. 2003/0037198 ("Hunsaker"). The Advisory Action of April 18, 2006 maintained the rejection and simply stated "Applicant's arguments are not persuasive" for the reason that the prior amendment did not place the application in condition for allowance. Appellant respectfully requests that the Examiner's rejection of claims 1-3, 5, and 21 based on Hunsaker be reviewed and reversed based on the following remarks.

Claim 1 calls for a bus controller having a memory interface to data memory and to a mass storage interface "without an intermediary mass storage controller." The claimed system provides a significant improvement over prior art systems, such as that shown in Figure 1 of Appellant's specification, because of the removal of the mass storage controller 103 and its additional interfaces and other complexities. Such an improvement is shown by way of example in the system of Figure 2, which shows a computing system having **a bus controller with an interface to** both data memory and **a mass storage interface** without a mass storage controller.

As discussed in Appellant's Amendments, Hunsaker shows a system in which the mass storage devices couple to the processor through 2 intermediate mechanisms, the MCH 130 and the ICH 150 as shown in Figure 1 of Hunsaker. In direct contrast, claim 1 calls for the "bus controller" to have "a memory interface coupled to the data memory and a mass storage device's interface **without an intermediary mass storage controller**." Neither the memory controller hub 130 nor the ICH 150 has both an interface coupled to the data memory and a mass storage interface so these devices cannot teach the bus controller of claim 1. The Office Action appears to be impermissibly combining the two controller hubs (MCH 130 and ICH 150) into a single controller as the Office Action states that the ICH 150 is coupled to system memory 140 via

MCH 130 and to mass storage device directly, which the Examiner feels meets the limitations of the bus controller of claim 1.

Appellant disagrees with this construction of the claim language of claim 1 and the teaching of Hunsaker. It is not proper to treat the combination of MCH 130 and ICH 150 as a single device as it is core to the Hunsaker device that these elements be implemented as separate devices. As such, they introduce a mandatory interface between the devices that must be traversed by mass storage transactions (similar to the additional interfaces of the mass storage controller 103 of Appellant's Figure 1). The invention of claim 1 eliminates this need for excessive interface traversal and therefore provides an improvement over the architecture of Hunsaker.

There are additional differences between the devices of Hunsaker and the bus controller of claim 1. Specifically, claim 1 requires that the bus controller has a memory interface "coupled to the date memory," and this is not taught by a connection via another controller (i.e., via MCH 130). Instead, Hunsaker would lead one skilled in the art to provide interfaces between the controllers 130 and 150 as is the case between the prior art controllers 101 and 103 shown in Applicant's Figure 1. Further, the MCH 130 would have the memory interface that is coupled to the system memory 140 not the ICH 150. But, the MCH 130 also cannot be the bus controller of claim 1 because it does not have a mass storage interface coupled to the mass storage device's interface.

The Response to Arguments on page 12 of the Final Office Action disagrees with the above argument. The Examiner states that the "ICH also directly interfaces with the memory hub controller 130, which is a memory interface." Then, the Examiner goes on to state that "Applicant has not shown why an interface to a memory controller is not a memory interface." Claim 1 calls for the bus controller to have "a memory interface coupled to the data memory." The Examiner states that ICH 150 directly interfaces with memory controller hub (MCH) 130 in Hunsaker's Figure 1. However, as discussed above, this is a controller to controller interface and does not teach an interface on the ICH 150 to system memory 140. All the interfacing functionality with system memory 140 in Hunsaker is provided by MCH 130 and not by the

interfaces between controllers 130 and 150. A person skilled in the art would be unlikely to construe an interface between controllers 130 and 150 to be a "memory interface coupled to the data memory" as called for in claim 1.

Further, paragraphs [0019] and [0020] of Hunsaker describe the ICH 150 as being more similar to the prior art bus controller 101 shown in Applicant's Figure 1 and not having the features of the bus controller of claim 1 (such as controller 201 of Applicant's Figure 2). Specifically, the ICH 150 is described as including a PCI bus interface and USB interfaces (as is the case with controller 101) that would enable it to interface with interfaces of a mass storage controller, such as controller 103 of Applicant's Figure 1. There is no description in these paragraphs regarding ICH 150 that there is or that it would be desirable to perform coupling directly with no mass storage controller provided in mass storage device 170 or that the ICH 150 is configured to "conduct mass storage transactions between the data memory and the mass storage device."

The Response to Arguments indicates that the Examiner did not find this argument persuasive because the "absence of discussion of there being no mass storage controller does not imply its presence." While this line of reasoning may hold some amount of weight, the absence of a discussion in Hunsaker regarding "a mass storage interface coupled to the mass storage device's interface" does imply that the controller or ICH 150 communicates with the mass storage device 170 in a standard manner or this is likely how one skilled in the art would construe such teaching. Otherwise, Hunsaker would have provided a discussion of an interface similar to the one described by Applicant. Because no discussion of the "mass storage interface" called for in claim 1 is provided in Hunsaker for the ICH 150, this reference does not explicitly teach or suggest such a direct interface as required under 35 U.S.C. §102 for an anticipation rejection (e.g., the only teaching of such an interface is Applicant's own specification and without such teaching a person reading Hunsaker would likely assume an interface more like that shown in Applicant's Figure 1). The Response to Arguments does not rebut Applicant's argument that the ICH 150 fails to include a mass storage interface coupled to the mass storage device's interface. For these reasons, Hunsaker fails to teach the bus controller of claim 1 and

does not anticipate the system of claim 1. Claims 2, 3, 5, and 21 depend from claim 1 and are believed allowable at least for the reasons provided for allowing claim 1 over Hunsaker.

Rejection of Claims 1, 12, and 20 Under 35 U.S.C. §102 Based on Zaidi Is Improper

In the February 10, 2006 Final Office Action, claims 1, 12, and 20 were rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Pat. No. 6,601,126 ("Zaidi"). The Advisory Action of April 18, 2006 maintained the rejection and simply stated "Applicant's arguments are not persuasive" for the complete reason that the prior amendment did not place the application in condition for allowance. Appellant respectfully requests that the Examiner's rejection of claims 1, 12, and 20 based on Zaidi be reversed based on the following remarks.

As discussed in several of Appellant's Amendments, Zaidi is cited by the Examiner in Fig. 28. However, in this illustration, Zaidi shows a computer architecture in which a bridge device, not a data/control bus, couples various components. There is no controller coupled to the CPU bus as called for in claim 1. Additionally, this figure of Zaidi fails to show or suggest a data memory coupled to the processor as called for in claim 1. Instead, the DRAM is coupled to the memory bus (m-bus). Moreover, Zaidi does not teach that its bridge is capable of conducting mass storage transactions between the data memory and the mass storage device as required of the bus controller of claim 1. Similarly, Zaidi does not teach that its MAC is capable of conducting mass storage transactions between the data memory and the mass storage device. For these reasons, claim 1 is not anticipated by Zaidi. Claims 12 and 20, which depend from claim 1, are allowable over Zaidi for at least the same reasons as claim 1.

In the Response to Arguments in the Final Office Action of February 10, 2006, the Examiner states that the remarks above provided by Appellant does not provide any evidence or well-reasoned logical arguments that certain limitations are not taught. This seems to be a shifting of the duty to show each and every limitation onto the Appellant – rather than simply providing an explanation of how each limitation is taught by the bridge of Figure 28. Further, Appellant disagrees that these remarks do not meet provide well reasoned arguments that show how Zaidi fails to anticipate claim 1. Specifically, Appellant's remarks provide references to

specific component cited by the Examiner in the rejection of the claims and explain why these components fail to shown the bus controller element of claim 1.

The Examiner has failed to make a *prima facie* case of anticipation because each and every element of the claim is not shown by Zaidi because the combination of the bridge and MAC do not meet the limitations of claim 1 for the bus controller (e.g., do not show a controller and do not show a controller that operates to conduct mass storage transactions between the data memory and mass storage). Further, the above arguments explain in detail how Zaidi fails to show the additional limitation of claim 1 that data memory be coupled to a processor. Hence, Appellant has fully complied with the requirements of 37 C.F.R. 1.111(b) in rebutting a rejection of claim 1 and requests that these arguments be fully considered and the rejection reversed.

Rejection of Claims 1, 14, and 20 Under 35 U.S.C. §102 Based on Moriarty Is Improper

In the February 10, 2006 Final Office Action, claims 1, 14, and 20 were rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Pat. No. 6,128,669 ("Moriarty"). Appellant respectfully requests that the Examiner's rejection of claims 1, 14, and 20 based on Moriarty be reversed based on the following remarks.

The Final Office Action cites Moriarty as teaching all the limitations of claim 1 in its Figure 1. However, in Figure 1, Moriarty shows a computer architecture in which a bridge device 106 is required for mass storage transactions. Hence, Moriarty does not show a bus controller that includes both a mass storage interface and an interface to the data memory as called for in claim 1. Instead, memory controller 108 enables memory transactions between the processor and the memory and a separate bridge 106 enables mass storage transactions. Hence, mass storage transactions must traverse multiple interfaces including the SCSI controller, PCI Bus, and Host bus.

In contrast, the multiple bus traversal required in the system of Moriarty's Figure 1 is minimized in the invention of claim 1. Specifically, claim 1 calls for the bus controller to include a memory interface coupled to the data memory, which is not shown as discussed above in Moriarty, and claim 1 calls for the bus controller to also include a mass storage interface

coupled to the mass storage device's interface, which is not shown by element 106 and 120 of Moriarty. Claims 14 and 20, which depend from claim 1, are allowable over Moriarty for at least the same reasons as claim 1.

The Response to Arguments again attempts to rebut these arguments by stating that they are not evidence or are not well-reasoned. Again, Appellant believes that the Examiner is not explaining how the Appellant's argument is incorrect and how the cited reference is useful as an anticipation rejection, but, instead, the Examiner is simply repeating a standard response to arguments that fails to rebut Appellant's arguments with regard to Moriarty. Appellant disagrees that the remarks are not adequate to overcome the Examiner's rejections based on Moriarty. Appellant has shown that the two interfaces required to be in the bus controller of claim 1 are not shown by Moriarty. The Response to Arguments also states that there is nothing in the claim elements that "precludes multiple bus traversals." However, claim 1 calls for the two interfaces of the bus controller to be coupled to the data memory and to the mass storage device's interface which eliminates a number of interfaces that would be required in the Moriarty system. Hence, Appellant has met his burden of specifically mapping the claim limitations to the deficiencies of Moriarty and its failure to anticipate or suggest at least the bus controller of claim 1. Again, the Advisory Action provided not response to these specific remarks but simply stated that the arguments were not persuasive, and the Examiner did not provide any reasoned arguments to address Appellant's characterization of Moriarty and the system of claim 1.

Rejection of Claims 1 and 19 Under 35 U.S.C. §102 Based on Ellison Is Improper

Still further, the Final Office Action rejected claims 1 and 19 under 35 U.S.C. §102(e) as being anticipated by U.S. Pat. Appl. Publ. No. 2002/0144121 ("Ellison"). Appellant requests that this rejection of claim 1 be reviewed and reversed based on the following remarks.

Claim 1 is believed allowable over Ellison at least for the reasons provided for allowing claim 1 over Hunsaker. The arguments provided for regarding Hunsaker are relevant to a rejection based on Ellison because the Examiner indicates that all the limitations of claim 1 are shown in Ellison's Fig. 1C, which provides teaching very similar to Hunsaker's Figure 1. Hence, these two references have similar failings relative to the system called for in claim 1.

More specifically, as discussed in Appellant's more recent amendments, Ellison shows a system in which the mass storage devices couple to the processor through an intermediate mechanism, the ICH 150. Neither the memory controller hub 130 nor the ICH 150 has both an interface coupled to the data memory and a mass storage interface. It is not proper to treat the combination of MCH 130 and ICH 150 as a single device as it is core to the Ellison device that these elements be implemented as separate devices. As such, they introduce a mandatory interface between the devices that must be traversed by mass storage transactions. The invention of claims 1 and 19 call for a single controller having a memory interface and a mass storage interface that eliminates this need for excessive interface traversal and therefore provides an improvement over the architecture of Ellison.

Further, the same Response to Arguments was applied to Appellant's arguments regarding Ellison as were provided for Hunsaker. As a result, the discussion provided regarding the Response to Arguments and the reasons for allowing claim 1 over Hunsaker are believed equally applicable to the use of Ellison in rejecting claim 1. Specifically, the Examiner seems to be asking to have it both ways by arguing that the ICH 150 could have both the interfaces called for in claim 1 although they are not shown or discussed in Ellison but the mass storage devices do not have an intermediary mass storage controller because none is shown (e.g., if Examiner is correct that the failure to discuss a mass storage controller means there is not one, then that is also true at least for the memory interface of the bus controller of claim 1 as a claimed element cannot just be presumed to exist in a reference even though no coupling between the ICH 150 and the system memory is shown). For all of these reasons, claim 1 and claim 19, which depends from claim 1, are believed allowable over Ellison.

Rejection of Claims 17 and 18 Under 35 U.S.C. §102 Based on Houston Is Improper

Additionally, the Final Office rejects claims 17 and 18, which depend from claim 1, under 35 U.S.C. §102(e) as being anticipated by U.S. Pat. No. 6,493,656 ("Houston"). Claim 1 is not, and has never been, rejected as being anticipated by Houston. Appellant requests that the rejection of claims 17 and 18 be reversed based on the following remarks.

The Office Action states that the bus controller of claim 1 is shown in Figure 1 of Houston by "102, or 114, or 102 and 114." Appellant argues that the bus controller of claim 1 is not shown by the controller 102 of Houston or by the combinations of 102 and 114 or 102 and 121. Claim 1 calls for the bus controller to interface with a mass storage device without a mass storage controller but such an intermediary storage controller would be the used with HDs of Houston, e.g., see Figure 2 and controller 214. Again, the only rebuttal of these arguments in the Response to Arguments was that arguments were not well-reasoned, but the arguments discuss the specifically-cited components of Houston and explain how these do not teach the bus controller of claim 1 and its two specific interfaces and their coupling. Hence, Appellant has provided arguments that if fully considered should overcome the rejections based on Houston.

Further, as discussed in the prior amendments, Houston shows a computer architecture that lacks a controller having a memory interface and a mass storage interface. North Bridge element 102, by itself, has only a memory interface and a PCI bus interface, not a mass storage interface. Accordingly, Houston does not show or fairly suggest the invention of claims 17 and 18 because it fails to show at least the bus controller of claim 1. Hence, claims 17 and 18 are allowable over Houston at least because Houston fails to anticipate independent claim 1 which is the base claim for claims 17 and 18 and the Examiner has never asserted that claim 1 is anticipated by Houston (except indirectly in the rejection of claims 17 and 18).

Rejection of Claims 7, 10, and 32 Under 35 U.S.C. §103 Based on Hunsaker, Zaidi, Moriarty, or Houston Is Improper

In the February 10, 2006 Final Office Action, the Examiner provided new claim rejections. The Office Action rejected claims 7, 10, and 32 under 35 U.S.C. §103(a) as being unpatentable over Hunsaker, Zaidi, Moriarty, or Houston in view of Tanenbaum. It is requested that the rejection of claims 7 and 10, which depend from claim 1, and independent claim 32 based on the following remarks.

Claims 7 and 10 depend from claim 1 and are believed allowable over Hunsaker, Zaidi, Moriarty, or Houston when considered alone for the reasons provided above for allowing claim 1 over each of these references. The addition of Tanenbaum to the teachings of these references

does not make claims 7 and 10 obvious because Tanenbaum fails to overcome the deficiencies of the base references with regard to claim 1.

Significantly, Tanenbaum had previously been cited by the Examiner (see, for example, the December 22, 2004 Office Action) as anticipating claim 1. Those rejections have been withdrawn because the reference did not show all the limitations of claim 1 and failed to support an anticipation rejection of claim 1. Further, the Examiner does not argue that Tanenbaum suggests each limitation of claim 1, and Tanenbaum is not being cited by itself as making the system of claim 1 obvious. Hence, Applicant requests that the rejection of claims 7 and 10 based on Hunsaker, Zaidi, Moriarty, or Houston in view of Tanenbaum be withdrawn.

More particularly, Tanenbaum fails to teach each and every limitation of claim 1 (or to at least teach the missing bus controller of claim 1). Tanenbaum does not teach the bus controller of claim 1 with its "Disk controller with DMA." This disk controller is a mass storage controller as shown in Applicant's Figure 1, and Tanenbaum fails to show a bus controller associated with its CPU that conducts mass storage transactions as called for in claim 1. Tanenbaum, therefore, does not overcome the base references' deficiencies because at least the bus controller configured as required by the language of claim 1 is not shown or even suggested by Tanenbaum.

Further, claim 1 calls for a data memory coupled to and shared by both the processor and the mass storage device. The disk controller in Tanenbaum is not a mass storage device as called for in claim 1 but is instead an interface to a mass storage device labeled "disk" in Tanenbaum, i.e., is a mass storage controller with such an interface. However, even if the disk controller were to be integrated with the disk in Tanenbaum, the reference shows a disk controller having memory (labeled "buffers") that is separate from and independent of the block labeled memory. Tanenbaum does not fairly suggest that the disk controller buffers could be implemented in the memory or that the memory could be implemented by the disk controller buffers, so as to provide a data memory coupled to and shared by both the processor and the mass storage device as called for in claim 1. For these additional reasons, claim 1 is allowable over the Tanenbaum reference when considered alone or in combination with the other four references. No rebuttal of

this description of Tanenbaum was provided in the Office Action in the Response to Arguments or in the Advisory Action. Hence, claims 7 and 10 are believed allowable as depending from allowable claim 1.

Independent claim 32 is directed to a system with some limitations similar to that of claim 1, and as a result, the reasons for allowing claim 1 over the four base references and Tanenbaum are believed applicable to claim 32. Further, claim 32 calls for a first mass storage device with an interface and the first mass storage device is coupled to a data/control bus. A processor is coupled to this same bus and implements mass storage control processes to control the first mass storage device. A second mass storage device with an interface is provided along with a bus controller that has a mass storage interface coupled to the second mass storage device's interface. Data memory is provided that is coupled to the data/control bus and the bus controller conducts mass storage transactions between the data memory and the second mass storage device. As can be seen, there are similarities between the system of claim 1 and claim 32, but the system of claims 32 calls for additional components and a specific arrangement not required in claim 1.

The Examiner does not address these additional limitations of claim 32 with reference to claim 1, and, as a result, **a *prima facie* case of obviousness has not yet been stated for claim 32** by the Office as the rejections of claim 1 based on Hunsaker, Zaidi, Moriarty, and Houston are directly applied to claim 32 without accounting for the different or additional components and their interfaces/couplings. Appellant requested in the April 4, 2006 Amendment that "the rejection of claim 32 be withdrawn or a proper case of obviousness be made with a showing of where each element in the claim is shown or suggested (e.g., the Office must show two mass storage devices, a data/control bus, a processor implement mass storage processes, and the bus controller as claimed in claim 32)." The Advisory Action did not address this request, and, as a result, a proper case of obviousness has not been presented by the Examiner, and Appellant requests that the rejection be reversed and withdrawn.

Conclusion

In view of all of the above, all of the pending claims are believed to be allowable and the case in condition for allowance. Appellant respectfully requests that the Examiner's rejections based on 35 U.S.C. §§102 and 103 be reversed for all the pending claims.

Respectfully submitted,

Date: July 24, 2006

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VIII. CLAIMS APPENDIX

1. A computing system comprising:

a processor having a data/control bus interface;

a data/control bus implementing one or more device communication channels;

a mass storage device having an interface for communicating mass storage transactions;

a data memory coupled to and shared by both the processor and the mass storage device; and

a bus controller having a memory interface coupled to the data memory and a mass storage interface coupled to the mass storage device's interface without an intermediary mass storage controller and operable to conduct mass storage transactions between the data memory and the mass storage device and to arbitrate access to memory locations within the data memory between the data/control bus and the mass storage device.

2. The computing system of claim 1 wherein the data memory is coupled to the processor by a memory bus operating independent of the data/control bus.

3. The computing system of claim 2 wherein the controller comprises a memory access controller coupled to the processor, the data memory, and the mass storage device and operable to arbitrate accesses to the data memory between the mass storage and the processor.

5. The computing system of claim 1 wherein the data memory is coupled to the data/control bus.

7. The computing system of claim 1 further comprising storage controller processes and application behavior processes implemented using the processor.

10. The computing system of claim 1 wherein the processor implements data structures storing physical geometry information about the mass storage device.

12. The computing system of claim 1 wherein the controller is integrated with the processor on a single integrated circuit chip.

17. The computing system of claim 1 wherein the mass storage device comprises:

a spinning disk having magnetic storage media provided on at least one surface;

a head for accessing data stored in the magnetic storage media;

an actuator mechanism for moving the head relative to the magnetic storage media in response to commands;

a servo controller coupled to the data memory and configured to generate the commands to the actuator mechanism.

18. The computing system of claim 17 wherein the mass storage device's interface is implemented by the servo controller and implements a physical interface to the data/control bus and a physical interface to the head and actuator mechanism.

19. The computing system of claim 1 wherein the computing system comprises a set-top box including processes for implementing audio/video behaviors in the processor.

20. The computing system of claim 1 wherein the computing system comprises a network appliance having a network controller coupled to the data/control bus.

21. The computing system of claim 1 wherein the mass storage device comprises an optical storage device.

22. The computing system of claim 1 wherein the mass storage device comprises a magneto-optical storage device.

32. A computing system comprising:

a data/control bus implementing one or more device communication channels;

a first mass storage device having an interface for communicating mass storage transactions, wherein the mass storage device is coupled to the data/control bus;

a data memory coupled to the data/control bus;

a processor having a data/control bus interface coupled to the data/control bus, wherein the processor implements mass storage control processes to control the mass storage device;

a second mass storage device having an interface; and

a bus controller having a mass storage interface coupled to the second mass storage device's interface and operable to conduct mass storage transactions between the data memory and the second mass storage device.

IX. EVIDENCE APPENDIX

No copies of evidence are required with this Appeal Brief. Appellant has not relied upon any evidence submitted under 37 C.F.R. §§ 1.130, 1.131, or 1.132.

X. RELATED PROCEEDINGS APPENDIX

There are no copies of decisions rendered by a court or the Board to provide with this Appeal as there are no related proceedings.